

EFFICIENT APPROACHES FOR DESIGNING REVERSIBLE BINARY CODED DECIMAL ADDERS

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ABSTRACT

Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low-power CMOS, nanocomputing and optical computing. This paper presents improved and efficient reversible logic implementations for Binary Coded Decimal (BCD) adder as well as Carry Skip BCD adder. It has been shown that the modified designs outperform the existing ones in terms of number of gates, number of garbage outputs, delay, and quantum cost. In order to show the efficiency of the proposed designs, lower bounds of the reversible BCD adders in terms of gates and garbage outputs are proposed as well.

Over the past few decades, improvements in fabrication and higher-level integration have led to better logic circuits and a marked decrease in energy loss. This pattern is The physical limit of heat reduction in computation also exists. Landauer asserts that in the calculation of logic, each bit of Heat energy equal to $kT \ln 2$ joules is produced by information loss.

1. INTRODUCTION:

The complexity of VLSI is being designed and used today makes the manual approach to design impractical. Design automation is the order of the day. With the rapid technological developments in the last two decades, the status of VLSI technology is characterized by the following

A steady increase in the size and hence the functionality of the ICs:

A steady reduction in feature size and hence increase in the speed of operation as well as gate or transistor density.

A steady improvement in the predictability of circuit behavior.

A steady increase in the variety and size of software tools for VLSI design.

The above developments have resulted in a proliferation of approaches to VLSI design.

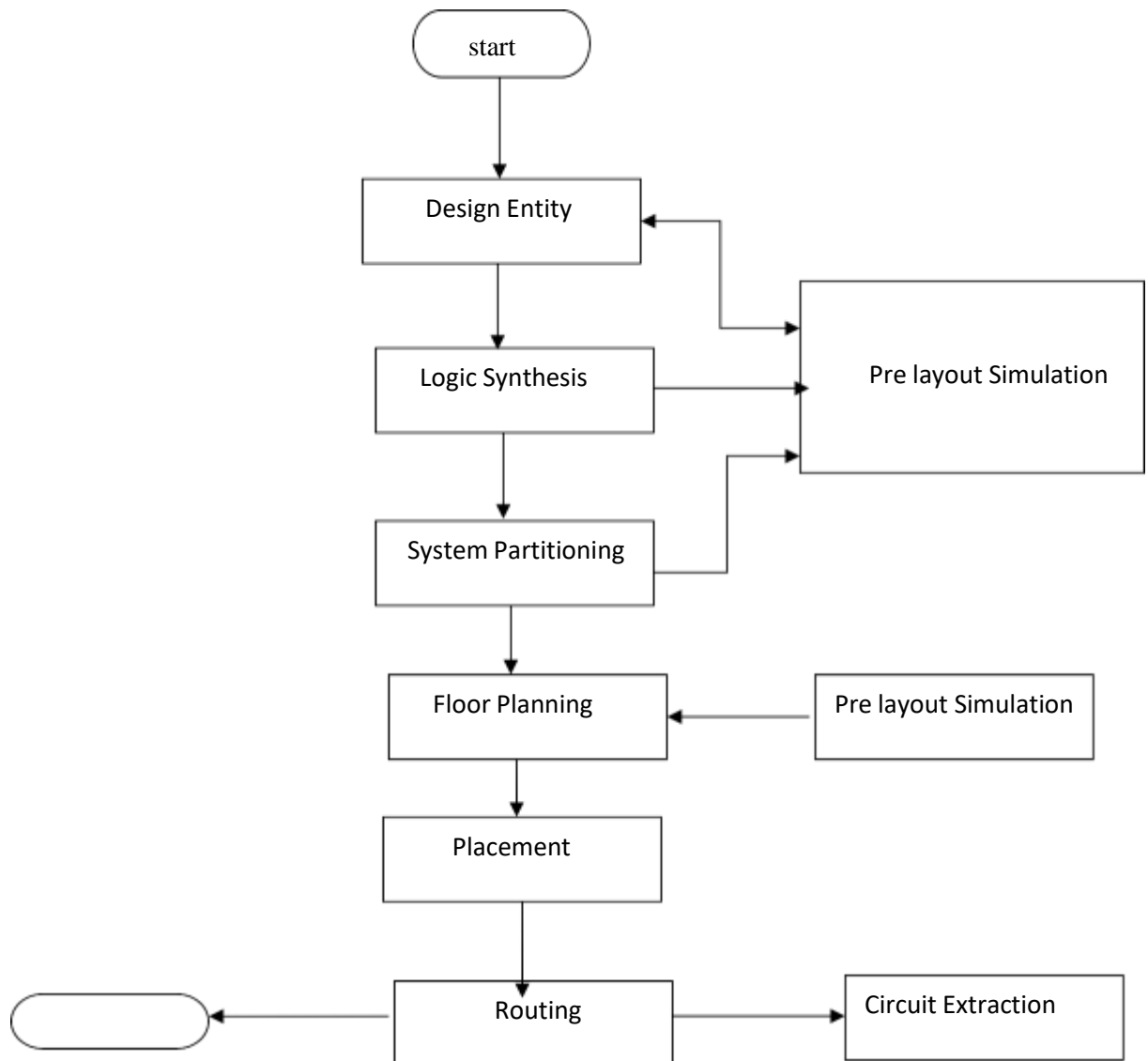
1.1 VLSI DESIGN FLOW:

Fig 1.1 VLSI Design Flow

2. BASIC DEFINITIONS OF REVERSIBLE LOGIC:

In this section, basic definitions and ideas related to reversible logic are presented. We formally define reversible gate, garbage output and present the popular reversible gates along with their input–output vectors. Illustrative figures and examples are also included in respective discussions. Definition 2.1. A Reversible gate is a k -input, k -output (denoted by $k \times k$) circuit that produces a unique output pattern [11,12] for each possible input pattern. Reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs, i.e., it can generate unique output vector from each input vector and vice versa. Example 2.1. Let the input vector be I_v , output vector O_v and they are defined as follows, $I_v = (I_1, I_2, I_3, \dots, I_k)$ and $O_v = (O_1, O_2, O_3, \dots, O_k)$. For each particular i , there exists the relationship $I_i \leftrightarrow O_i$. Definition 2.2. Unwanted or unused output of a reversible gate (or circuit) is known as Garbage Output. More formally, the outputs, which are needed only to maintain reversibility, are called garbage outputs. Example 2.2. If we wish to perform Exclusive-OR between two inputs, we can use the Feynman gate (FG) [13], but in that case, one extra output will be generated as well, which is the garbage output in this regard. The garbage output of Feynman gate is shown in Fig. 1 with A . Definition 2.3. The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the following assumptions: (i) Each gate performs computation in one unit time. (ii) All inputs to the circuit are available before the computation begins.

3. QUANTUM ANALYSIS OF DIFFERENT REVERSIBLE LOGIC GATES:

Calculating quantum cost of reversible circuit is always an interesting topic. Quantum circuits [3], DNA technologies [6], nanotechnologies [5] and optical computing [7] are the most common applications of quantum theory. Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. Reducing the quantum cost from reversible circuit is always a challenging one and works are still going on in this area. In this section, we will show the quantum equivalent diagram of each reversible gates shown in Section 2 that will be used to calculate the final quantum cost of proposed reversible BCD adder and reversible Carry Skip BCD adder. Definition 3.1. The quantum cost of every 2×2 gate is the same [22]. We can easily assume that a 1×1 gate costs nothing, since it can be always included to arbitrary 2×2 gate that precedes or follows it. Thus, in

first approximation, every permutation quantum gate will be built from 1 1 and 2 2 quantum primitives and its' cost calculated as a total sum of 2 2 gates used. All gates of the form 2 2 have equal quantum cost and the cost is unity. Example 3.1. Reversible NOT gate: Since this is a 1 1 gate, the quantum cost is 0. Example 3.2. Feynman gate: A 2 2 FG is also called CNOT. This gate is one through because it passes one of its inputs. Every linear reversible function can be built by using only 2 2 FG and inverters. Since this is a 2 2 gate, the quantum cost is 1. Quantum equivalent circuit of FG is shown in Fig. 3.1.

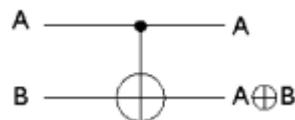


Fig. 3.1. Quantum equivalent circuit for Feynman gate

4. DESIGN ANALYSIS OF EXISTING TECHNIQUES:

In reversible synthesis, some facts should be kept in mind that, reversible synthesis is strikingly different from the irreversible ones. Before discussing about the realization of BCD adders, it is good to have a look at the differences: In reversible logic, fan-out of any gate output is strictly restricted. We can use any output only once. If we need to use the output more than once, copying circuit should be used. FG is an optimal way for increasing fan-out; the same way as in “spy circuit”, but adding a FG increases delay and complexity of the circuit. A design technique for reversible BCD adder is presented in Ref. [9], where the basic features of this design are the use of combination of New gate [20] and Peres gate as full-adder, one 4-bit parallel adder to get the result of the binary addition of two BCD numbers, a combinational circuit to detect BCD overflow and a 4-bit parallel adder for error correction if overflow occurs. The design techniques for both reversible BCD adder and Carry Skip BCD adder are presented in Ref. [10] and one of the basic characteristics of these designs is the use of TSG gate as a full adder. For reversible BCD adder, one 4-bit parallel adder is used for binary addition of the numbers, a combinational circuit is used for detection of BCD overflow and another 4-bit parallel adder is used for error correction. For Reversible Carry Skip BCD adder, carry skip logic is incorporated for faster carry generation, which is used in the overflow detection logic. Other basic components are same as reversible BCD adder. The general ideas of these designs are as follows: in the first 4-bit parallel adder, initial sum is produced by the binary addition of the two BCD numbers. In the combinational part, BCD overflow is detected. In the strict reversible sense, fan-out is restricted. Therefore, copying circuit is used. In the correction part, a 4-bit parallel adder is used to add the error correction value, i.e., in binary 0110, whenever overflow occurs. Otherwise, output

produced by the first 4-bit parallel adder becomes the final output. However, there are scopes to improve the designs in terms of number of gates, garbage outputs, gate complexity and delay. We have proposed the design of reversible BCD adder and Carry Skip reversible BCD adder, which overcome the limitations of the existing designs.

5. PROPOSED REVERSIBLE BCD ADDERS:

In this section, improved designs for reversible BCD and Carry Skip reversible BCD adders have been presented.

5.1. Basic properties

In this section, definitions and necessary terminologies relating to BCD number and adder are presented.

Definition 5.1.1. A full-adder is a device that takes two input bits with a carry-in (C_{in}) bit and produces the output with sum of the bits and the carry-out (C_{out}). **Example 5.1.1.** There are several other full-adder designs in the literatures [11,12,16,18,19]. The design we use [18,19] is shown in Fig. 15, which uses only one gate and better than the existing ones. Lower bound in terms of number of gates is presented in **Theorem 5.1.1.** **Theorem 5.1.1.** A reversible full adder can be realized by at least one gate. **Proof.** The input and output vector, I_v and O_v for reversible MTSG gate are (A, B, C, D) and $(P \frac{1}{4} A, Q \frac{1}{4} A$

B,	R	$\frac{1}{4}$
(A		
B		
C),	and	S
(A		$\frac{1}{4}$
B)C		
AB		

D, respectively. If we put input bit, $D \frac{1}{4} 0$ (constant) and other 3 inputs are for the 3 bits to be added; sum and carry are produced at output R and S, respectively; and hence, a reversible full adder can be realized by at least one gate.



Fig. 5.1. A full-adder using a 4 4 MTSG gate.

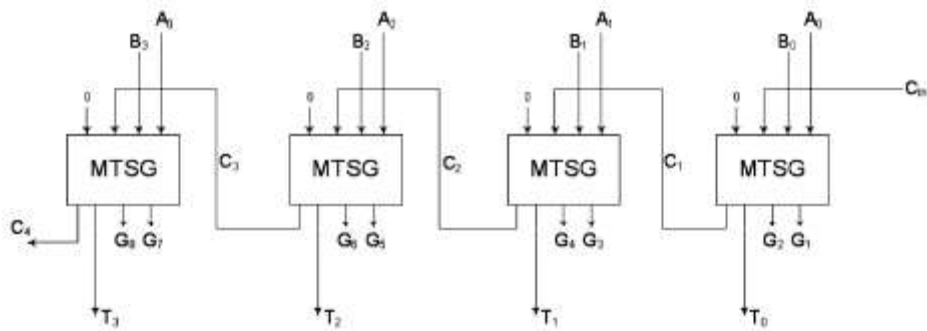


Fig. 5.2. Designing a 4-bit binary adder using MTSG reversible gate.

A Carry Skip reversible BCD adder consists of the following components: a 4-bit parallel adder, Carry Skip logic, BCD adder overflow detection logic and BCD adder overflow correction logic. Carry Skip logic may generate the carry out (C_{out}) instantaneously. We will present these components with proper algorithms and appropriate figures. A design for Carry Skip reversible BCD adder was presented in Ref. [10]. But the proposed design to be discussed in this section is better than the existing one in terms of number of gates, number of garbage, delay, and quantum cost. Note that the proposed carry skip reversible BCD adder also performs better in terms of number of gates and quantum cost than the carry skip reversible BCD adder which is implemented using HNG gate [27] instead of the proposed MTSG gate. Carry Skip logic circuit is the fundamental part to this design. We can propagate the carry in, C_{in} to the carry-out, C_{out} of the block. Let, A_i and B_i be the inputs to i th full-adder and either of them is set.

Propagation $P_i \frac{1}{4}$

A_i

B_i and C_{in} to the block will propagate to the carry output of the block if the entire P_i 's are set. In this way, we can generate C_{out} without waiting for it to be generated in ripple carry fashion. Let, the propagation signal for the block is denoted by P . If P is set, C_{in} will be propagated to the C_{out} . However, in the other case, C_{out} will be generated in the ripple carry fashion. So, carry skip logic bit of the block is $K \frac{1}{4} PC_{in} + C_4$ where C_4 is the carry generated in the ripple carry fashion. K can be slightly modified to realize the logic more clearly: $K \frac{1}{4} PC_{in}$

PC^{-4} —the expression reveals the fact that if P (Propagate) is true, we do not have to wait for the generation of final carry out C_4 , but if P is false, we need to go in formal way, i.e., wait for C_4 to generate. The overall overflow detection bit, $F \frac{1}{4} (T_1 + T_2)$

T_3

6

K is generated in the same way with reversible BCD adder presented earlier in this paper.

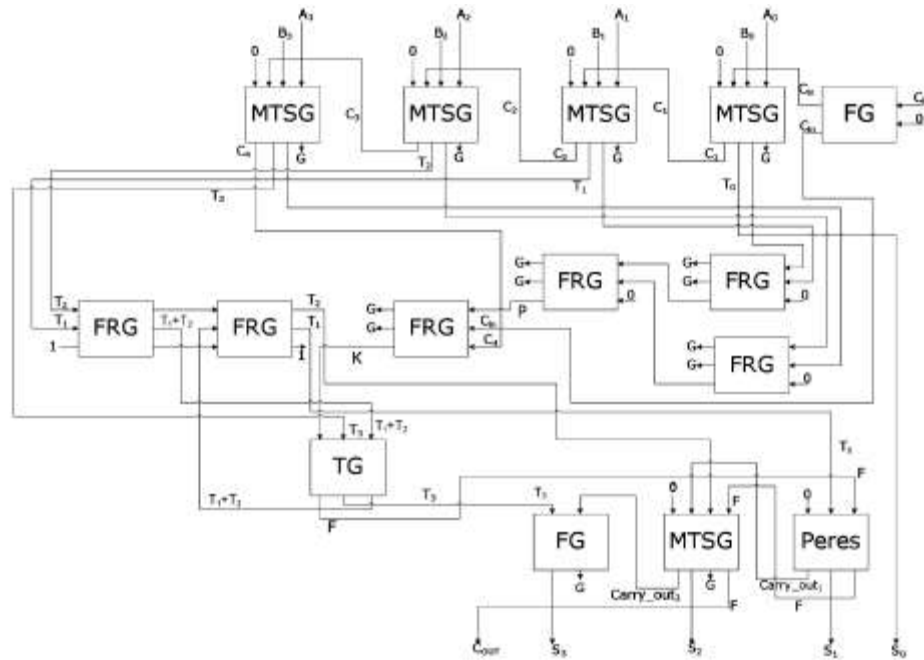


Fig. 5.3. Design of a Carry Skip 1-digit BCD adder.

6. CONCLUSION:

In this paper, reversible logic syntheses were carried out for both Binary Coded Decimal (BCD) adder and Carry Skip BCD adder. The designs have been developed for ease of reversible logic implementation and it has been found that the proposed designs are far better than the existing ones in terms of number of gates needed, number of garbage outputs produced and delay required. Improved Carry Skip BCD adder can perform much faster than the existing BCD adder. Moreover, quantum costs for the proposed circuits are much less than the existing designs. If multiple BCD blocks are used, i.e. m-digit BCD numbers then Carry Skip BCD adder has the potential to perform the desired operations much faster. BCD adders can be an important part of some other larger and more complex reversible circuits [13–15]. Fast and improved BCD adders may also find its use in future quantum computers.

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